**DSD LAB REPORT**

# LAB # 02



# Spring 2021

[**CSE-308L Digital System Design Lab**](https://classroom.google.com/u/0/c/MzA5OTAyNzE2MzM2)

Submitted by: **Hurair Mohammad**

Registration No. : **18PWCSE1657**

Class Section: **B**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

# Engr. Madiha Sher

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

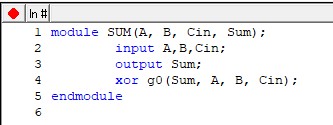
**OBJECTIVES:**

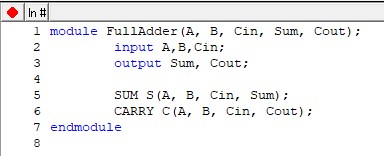
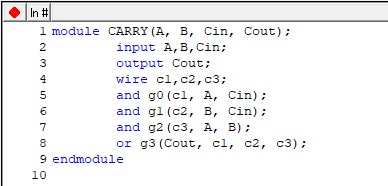
* Learn top down and bottom up design methodologies
* Data flow level modeling

**TASK01 (a):**

**CODE:**

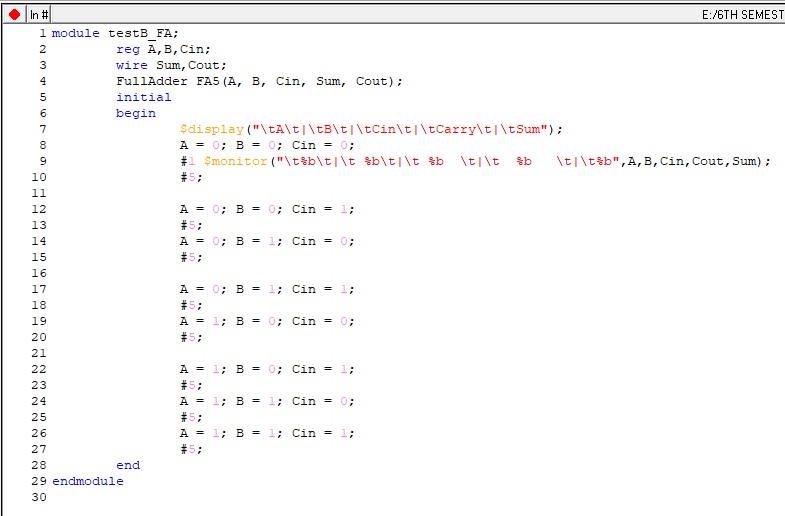
**Step1:**



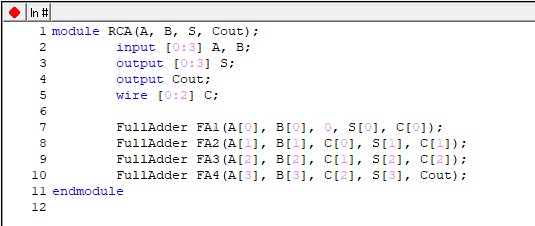


**Step2:**

**TestBench:**

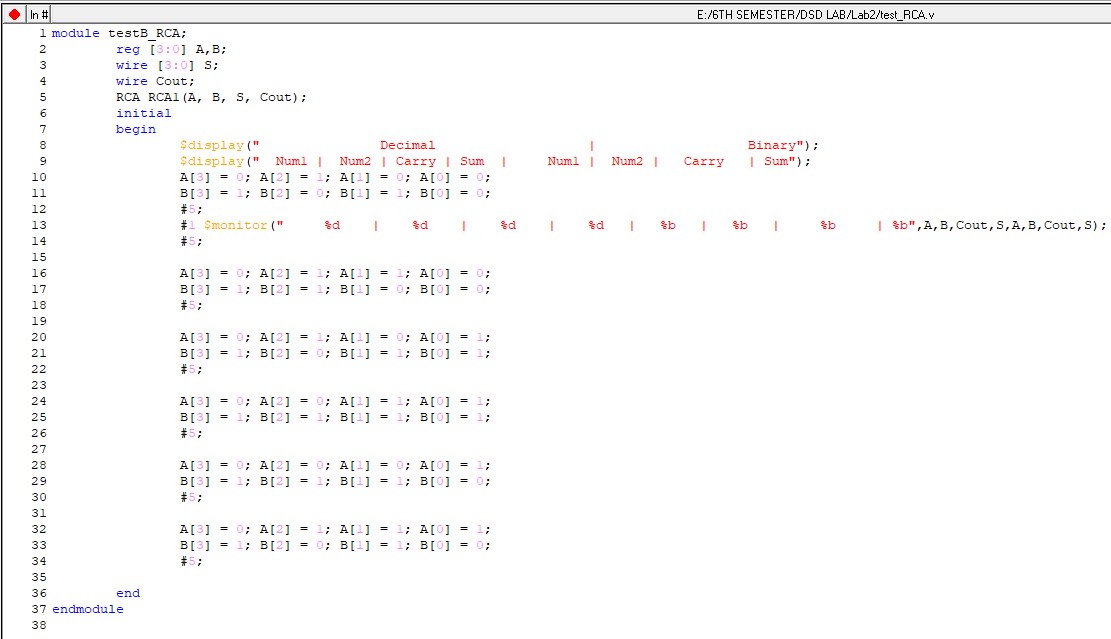


**Step3:**



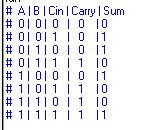
**Step4:**

**TestBench:**

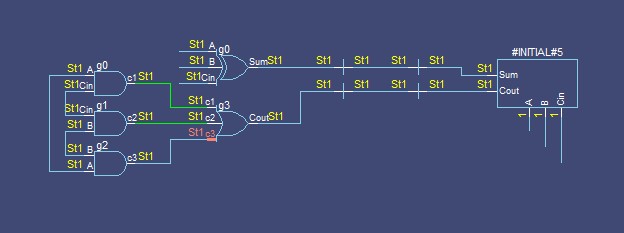


**OUTPUTS FULL ADDER:**

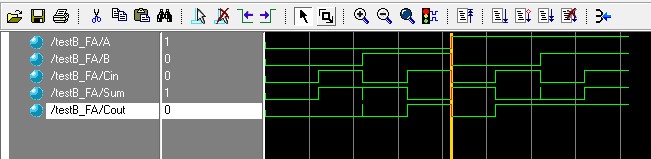
**Truth Table:**



**Circuit Design:**

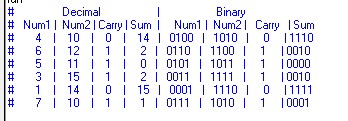


**Wave Form:**

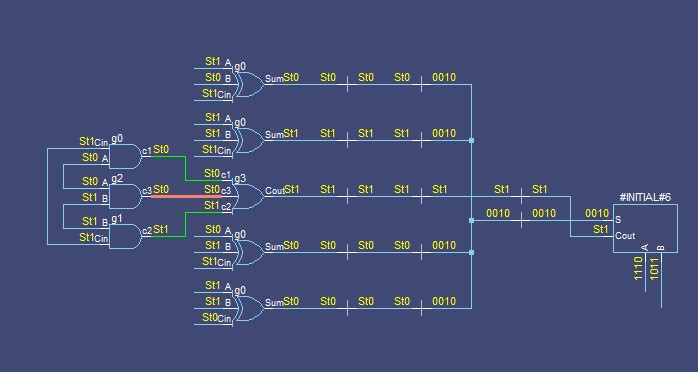


**RIPPLE CARRY ADDER:**

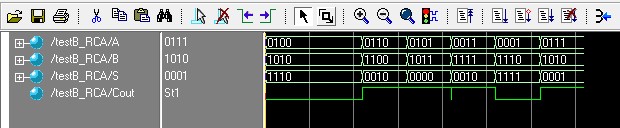
**Truth Table:**



**Circuit Design:**



**Wave Form:**

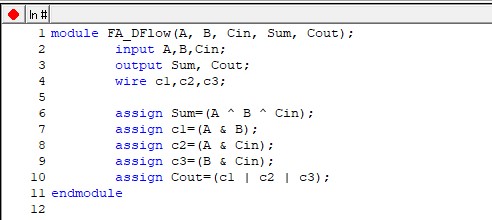


**TASK01 (b):**

Design the 4-bit full adder using data flow level modeling.

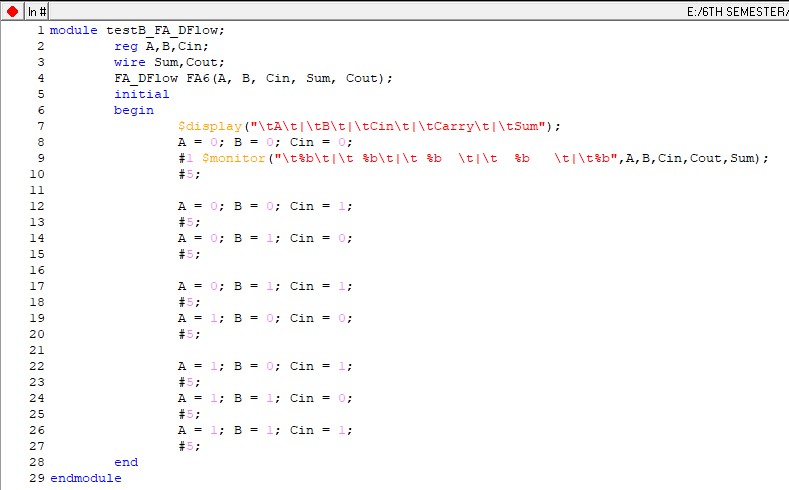
**Step1:**

**CODE:**

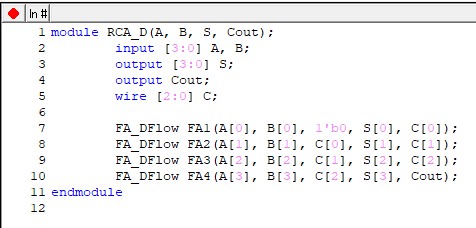


**Step2:**

**TestBench:**

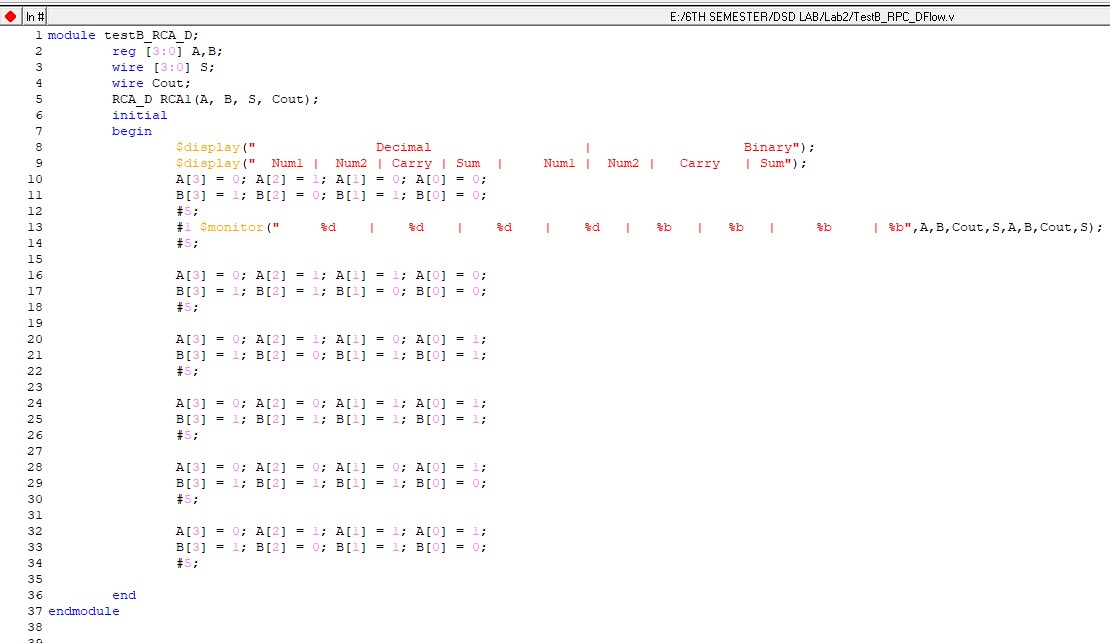


**Step3:**



**Step4:**

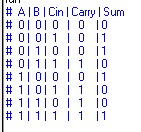
**TestBench:**



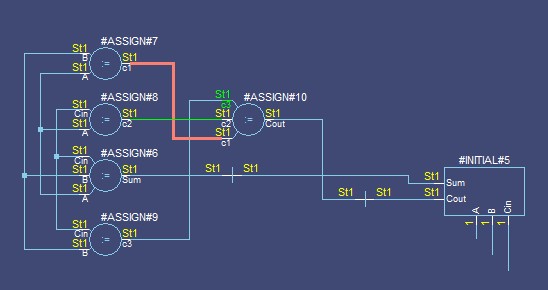
**OUTPUTS**

**Full Adder:**

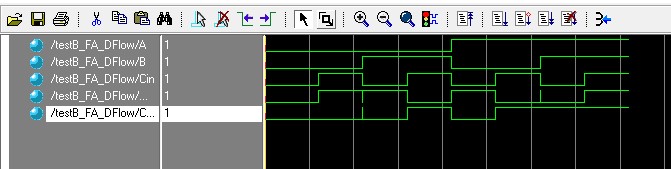
**Truth Table:**



**Circuit Design:**

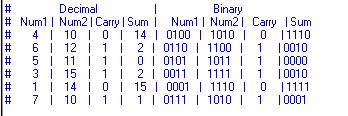


**Wave Form:**

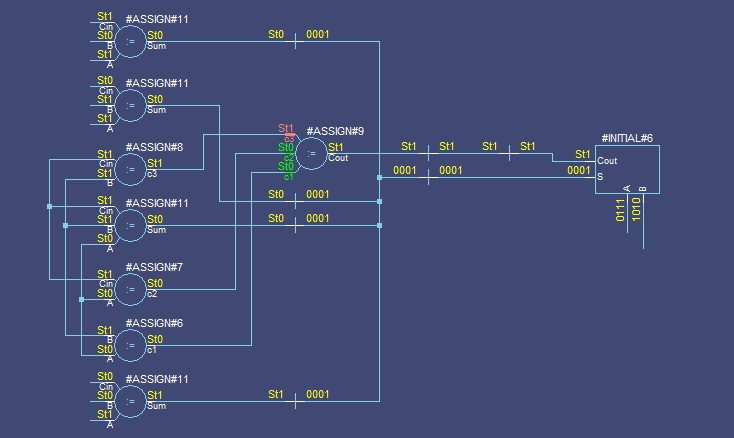


**Ripple Carry Adder:**

**Truth Table:**



**Circuit Design:**



**Wave Form:**

